Drafts
Pending
Active
    L4: (209) (("4782439" or "5388229" or "5583964" or "5740325" or "5822616") o
Failed
Saved
    S1: (29151) dma
    S2: (41) push near9 S1
    S3: (0) S1 near9 S1 near9 to
    S4: (7248) S1 near9 S1
    S5: (5456) S1 near5 S1
    S6: (0) S4 near9 to
    S7: (0) dma near9 to
    S8: (2610) (controller processor) near9 S5
    S9: (153023) data near9 bus
    S10: (382) S8 with S9
    S11: (456) master near9 slave near9 S1
    S12: (242) (controller processor) near9 S11
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BRS form   IS&R form   Image   Text   HTML

	U	✓	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classi	I
1	☐	☑	US 5652915 A	19970729	11	System for controlling mode of operation of a data cache based on	710/52	711/123; 711/142		Jeter; Jay D.
2	☐	☑	US 5257374 A	19931026	46	Bus flow control mechanism	718/105	709/212; 709/226		Hammer; Wil
3	☐	☑	US 5768557 A	19980616	20	Low cost writethrough cache coherency apparatus and method for	711/146	711/135		Kulkarni; Upe
4	☐	☑	US 5430847 A	19950704	23	Method and system for extending system buses to external devices	710/310	710/308		Bradley; Jose
5	☐	☑	US 5590377 A	19961231	14	Automatic control of distributed DMAs in a PCI bus system supporting dual ISA	710/22	710/28; 710/303;		Smith; Micha
6	☐	☑	US 5664142 A	19970902	9	Chained DMA devices for crossing common buses	711/112	710/22; 711/163		Boldt; Gerald

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